

AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

- 1.(withdrawn) A semiconductor device having a non-volatile memory transistor, the semiconductor device comprising:
- an interlayer dielectric layer provided on a semiconductor layer in which the non-volatile memory transistor is formed,
- wherein the interlayer dielectric layer is an insulation layer for electrically isolating the non-volatile memory transistor from a conductive layer formed over the semiconductor layer, and the interlayer dielectric layer includes a layer containing nitride.
- 2.(withdrawn) A semiconductor device according to claim 1, wherein the layer containing nitride is provided as a lowermost layer of the interlayer dielectric layer.
- 3.(withdrawn) A semiconductor device according to claim 1, wherein the layer containing nitride is provided as an uppermost layer of the interlayer dielectric layer.
- 4.(withdrawn) A semiconductor device according to claim 1, wherein the layer containing nitride is provided as an intermediate layer of the interlayer dielectric layer.

5.(withdrawn) A semiconductor device according to claim 1, wherein the nitride is at least one of silicon nitride and silicon oxide nitride.

6.(withdrawn) A semiconductor device according to claim 1, wherein the non-volatile memory transistor includes:

a floating gate disposed over the semiconductor layer through a gate dielectric layer;

a tunneling dielectric layer that contacts at least a part of the floating gate;

a control gate that is formed over the tunneling dielectric layer; and source region and drain region formed in the semiconductor layer.

7.(withdrawn) A semiconductor device according to claim 1, wherein the non-volatile memory transistor includes:

a floating gate disposed over the semiconductor layer through a gate dielectric layer;

a control gate disposed over the floating gate through an intermediate dielectric layer; and

source region and drain region formed in the semiconductor layer.

8.(currently amended) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor with the interlayer dielectric layer being in direct contact with a component of the non-volatile memory transistor,

a wiring layer provided on the interlayer dielectric layer,

wherein the interlayer dielectric layer includes an oxide film provided as a lowermost layer of the interlayer dielectric layer and a layer containing nitride provided on the oxide film.

9.(original) A semiconductor device according to claim 8, wherein the oxide film has a thickness of 10 – 80nm.

10.(original) A semiconductor device according to claim 8, wherein the oxide film has a thickness of 30 – 70nm.

11.(original) A semiconductor device according to claim 8, wherein the oxide film is an oxide film that is formed by a reduced pressure CVD method using TEOS.

12. – 18. (cancelled)

19.(new) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor, the non-volatile memory transistor having a split gate structure,

wherein the interlayer dielectric layer includes an oxide film layer and a layer containing nitride provided on the oxide film.

20.(new) A semiconductor device having a non-volatile memory transistor formed on a semiconductor layer, the semiconductor device comprising:

an interlayer dielectric layer provided over the semiconductor layer and the non-volatile memory transistor,

wherein the interlayer dielectric layer includes an oxide film layer and a layer containing nitride provided on the oxide film and the oxide film layer has a thickness of 10 – 80 nm.

21.(new) A semiconductor device according to claim 20, wherein the oxide film has a thickness of 30 - 70 nm.